ENTITY ASMExample IS
  PORT (  Clock, Resetn, InBit, BufFull : IN  STD_LOGIC ;
          state      :  BUFFER STD_LOGIC_VECTOR (1 DOWNTO 0);
          CountEN, RegLD, OutFlag  : OUT  STD_LOGIC ) ;
END ASMExample ;

ARCHITECTURE ASMArch OF ASMExample IS
  CONSTANT A : STD_LOGIC_VECTOR (1 DOWNTO 0):= "10";
  CONSTANT B : STD_LOGIC_VECTOR (1 DOWNTO 0):= "11";
  CONSTANT C : STD_LOGIC_VECTOR (1 DOWNTO 0):= "00";
  CONSTANT D : STD_LOGIC_VECTOR (1 DOWNTO 0):= "01";

  SIGNAL nextState: STD_LOGIC_VECTOR (1 DOWNTO 0);

BEGIN
  PROCESS ( Resetn, Clock ) -- State transitions
  BEGIN
    IF Resetn = '0' THEN
      state <= A ;
    ELSIF (Clock'EVENT AND Clock = '1') THEN
      state <= nextState;
    END IF;
  END PROCESS ;
PROCESS (state, InBit, BufFull) -- conditional and uncond. Outputs, next state
BEGIN -- All outputs are default to '0'
  CountEN <= '0';
  RegLD <= '0';
  OutFlag <= '0';
  CASE state IS
    WHEN A =>
      CountEN <= '1';
      RegLD <= '1';
      IF InBit = '0' THEN nextState <= B ;
      ELSE nextState <= C ;
      END IF ;
    WHEN B =>
      nextState <= A;
    WHEN C =>
      RegLD <= '1';
      IF BufFull = '1' THEN
        CountEN <= '1';
        nextState <= D;
      ELSE
        nextState <= C;
      END IF ;
    WHEN D =>
      OutFlag <= '1';
      nextState <= A;
    WHEN OTHERS =>
      nextState <= A;
  END CASE ;
END PROCESS ;
END ASMArch ;